Remarks

Reconsideration of this Application is respectfully requested.

Claims 20-29 are pending in the application, with claims 20 and 25 being the independent claims. Claim 25 has been amended to correct a grammatical error therein. This change is believed to introduce no new matter, and its entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 20-29 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,041,738 to Walters, Jr. ("Walters").[1] Applicants have carefully considered the Examiner's rejections but, for the reasons set forth below, respectfully traverse.

Walters is directed to a CMOS clock generator that generates two CMOS phase clock signals having an adjustable overlap voltage. *See* Walters, col. 1, ll. 6-10. The clock generator 8 includes a first phase clock generating circuit 18 and a second phase clock generating circuit 22. *Id.*, col. 2, ll. 51-54, FIG. 1.

---

[1] In the second paragraph of the Office Action, the Examiner refers to U.S. Patent No. 5,041,990 to Walters, Jr. U.S. Patent No. 5,041,990 is a patent entitled "Method and Apparatus for Measuring Entrained Gas Bubble Content of Flowing Fluid" having an inventive entity of Yabumoto *et al.* Applicants have therefore assumed that the Examiner is referring to U.S. Patent No. 5,041,738 to Walters, Jr., which is prior art cited in Applicants' PTO-1449.

In Walters, the overlap voltage between the two CMOS phase clock signals is adjusted by selectively eliminating transistors in either or both of the first and second phase clock generating circuits 18 and 22. Transistors are eliminated by blowing fuses using a laser cut. *Id.*, col. 3, ll. 18-21, 51-54. The selective elimination of transistors determines the rate at which an internal node within the first and second phase clock generating circuits 18 and 22 can charge or discharge, which in turn, affects the rate at which the CMOS phase clock signals transition between high and low output levels.

In particular, Walters teaches that to decrease the amount of overlap voltage, one or more transistors connected in parallel between an internal node of a phase clock generating circuit and ground may be eliminated, and, when all such transistors have been eliminated, one or more transistors connected in parallel between the internal node and the clock output of the other phase clock generating circuit may be eliminated until only one such transistor is remaining. *Id.*, col. 6, ll. 37-64. Alternatively, to increase the amount of overlap voltage, one or more transistors connected in parallel between the internal node of a phase clock generating circuit and the clock output of the other phase clock generating circuit may be eliminated. *Id.*, col. 6, l. 64-col. 7, l. 19.

The clock generator circuit described in Walters has a very different topology than that disclosed and claimed in the present application. As a result, the manner in which overlap between the phase clocks signals is adjusted in Walters is also very different from that disclosed and claimed in the present application.

For example, claim 20 of the present application is directed to a method for manufacturing a clock generator that generates two non-overlapping clock signals that includes:

> providing an apparatus that includes a clock input portion, first and second clock outputs, ***a first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion***; . . . and
>
> ***adding one or more delay elements to said first and/or second feedback paths*** if said first and second clock signals do not have clock edges that are non-overlapping for said predetermined time T.

(Emphasis added).

Walters does not teach or suggest "providing an apparatus that includes . . . a first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion" as recited in claim 20. The Examiner has indicated that the recited first and second feedback paths correspond to lines 24 and 26 depicted in FIG. 1 of Walters. However, neither line 24 nor line 26 couples a clock output to the portion of clock generator 8 that receives the clock input (CLK) 12. Rather, lines 24 and 26 couple a clock output to an internal node within phase clock generating circuits 22 and 18, respectively.

Furthermore, even if lines 24 and 26 were deemed to be first and second feedback paths within the meaning of claim 20, Walters does not teach or suggest "adding one or more delay elements to said first and/or second feedback paths." Nowhere in Walters is it suggested to add elements that delay a signal along lines 24 or 26. Rather, as noted above, Walters teaches eliminating transistors coupled in parallel between an internal node of a phase clock generating circuit and ground and/or eliminating transistors connected in parallel between the internal node and the clock output of the other phase clock generating circuit. By varying the ratio between each type of transistor, the charge/discharge rate of an internal node within the first and second phase clock

generating circuits 18 and 22 can be controlled, which in turn, controls the rate at which the CMOS phase clock signals transition between high and low output levels.

Since Walters does not teach or suggest each and every limitation of claim 20, it cannot anticipate that claim. Accordingly, the Examiner's rejection of claim 20 under 35 U.S.C. § 102(b) is traversed and Applicants respectfully request that the rejection be withdrawn. Furthermore, dependent claims 21-24 are also not anticipated by Walters for at least the same reasons as independent claim 20 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 21-24 under 35 U.S.C. § 102(b) is also traversed and Applicants respectfully request that the rejection be withdrawn.

Claim 25 of the present application is directed to a method for manufacturing a clock generator that generates two non-overlapping clock signals that includes:

> providing an apparatus that includes a clock input portion, first and second clock outputs, ***a first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion***; . . . and
>
> ***removing one or more delay elements from said first and/or second feedback paths*** if said first and second clock signals do not have clock edges that are non-overlapping for said predetermined time T.

(Emphasis added).

As discussed above, Walters does not teach or suggest "providing an apparatus that includes . . . a first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion" as recited in claim 25. Furthermore, even if lines 24 and 26 from FIG. 1 of Walters were deemed to be first and second feedback paths within the meaning of claim 25, Walters does not teach or suggest "removing one or more delay elements

from said first and/or second feedback paths." Nowhere in Walters is it suggested to remove elements that delay a signal along lines 24 or 26.

Since Walters does not teach or suggest each and every limitation of claim 25, it cannot anticipate that claim. Accordingly, the Examiner's rejection of claim 25 under 35 U.S.C. § 102(b) is traversed and Applicants respectfully request that the rejection be withdrawn. Furthermore, dependent claims 26-29 are also not anticipated by Walters for at least the same reasons as independent claim 25 from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 26-29 under 35 U.S.C. § 102(b) is also traversed and Applicants respectfully request that the rejection be withdrawn.

Rejections under 35 U.S.C. § 103

The Examiner has rejected claims 22-24 and 27-29 under 35 U.S.C. § 103(a) as being unpatentable over Japanese Patent JP 2-124627 to Tazaki ("Tazaki") in view of Walters.[2] Applicants have carefully considered the Examiner's remarks but, for the following reasons, respectfully traverse.

Tazaki is directed to a clock driver circuit for obtaining complementary clock signals having a variable delay time. In particular, Tazaki teaches a clock driver circuit that includes two delay time selection circuits 5 and 8 having control terminals 6 and 9, respectively. *See* Tazaki, FIG. 1. Each delay time selection circuit 5 and 8 includes a decoder circuit 18, switches 16 and 17, and delay circuits 13, 14 and 15. *See* Tazaki,

[2] Applicants have obtained an English language translation of Tazaki, a copy of which has been submitted in an Information Disclosure Statement filed along with this Amendment and Reply.

FIG. 3. Control signals 9 are applied to decoder circuit 18 during operation of the device to controls switches 16 and 17 within the delay time selection circuit to either connect to or short-circuit delay circuits 13 and 14, respectively.

In contrast to the programming-based technique taught by Tazaki, which is implemented during operation of the device, the present invention uses a manufacturing-based technique to ensure generation of two non-overlapping clock signals. In particular as recited in claims 20 and 25, the present invention is directed to a "***method for manufacturing*** a clock generator that generates two non-overlapping clock signals." (Emphasis added). The method includes "adding one or more delay elements" (claim 20) or "removing one or more delay elements" (claim 25) from feedback paths of an apparatus during manufacturing. This feature is neither taught by Tazaki, which as illustrated above is directed to a programming-based technique for determining delay time between two clocks, nor by Walters, which as illustrated above, neither teaches feedback paths or adding/removing delay elements to feedback paths.

Since neither Tazaki nor Walters teach this claimed feature, the combination of these two references cannot support a prima facie obviousness rejection of independent claims 20 or 25. Consequently, dependent claims 22-24 and 27-29 are also not rendered obvious by this combination for at least the same reasons as the independent claims from which they depend and further in view of their own respective features. Accordingly, the Examiner's rejection of claims 22-24 and 27-29 under 35 U.S.C. § 103(a) is traversed and Applicants respectfully request that the rejection be withdrawn.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Thomas C. Fiala
Attorney for Applicants
Registration No. 43,610

Date: 8/2/04

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600